IN THE CLAIMS

1. **(Currently Amended)** A semiconductor circuit designing apparatus, comprising:

a circuit design unit which executes a logical design of a semiconductor integrated circuit; and

an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to ~~an~~ at least one inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates ~~target~~ circuit feature information indicating said circuit feature ~~of a target semiconductor integrated circuit~~ of said semiconductor integrated circuit for which said logical design should be executed,

wherein said circuit design unit obtains a ~~target~~ certain inspection item of said at least one inspection item corresponding to said ~~target~~ circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said ~~target~~ semiconductor integrated circuit in reference to said ~~target~~ certain inspection item.

2. **(Currently Amended)** A semiconductor circuit designing apparatus, comprising:

a circuit design unit which executes a logical design of a ~~smeiconductor~~ semiconductor integrated circuit; and

an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to ~~an~~ at least one inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates ~~a target~~ circuit feature information indicating said circuit feature ~~of a target semiconductor integrated circuit~~ for said semiconductor integrated circuit ~~of~~ for which said logical design should be executed,

wherein said circuit design unit obtains a ~~target~~ certain inspection item of said at least one inspection item corresponding to said target circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said ~~target~~ semiconductor integrated circuit in reference to said ~~target~~ certain inspection item, and further comprising:

a model development history database section in which ID data of said circuit design unit is stored corresponding to a number of times said circuit design unit failed said inspection of each one of said at least one inspection item previously,

wherein said ~~target~~ certain inspection item is determined such that ~~said~~ an inspection item of said at least one inspection item for which said number of times is smaller than a predetermined value is withdrawn from said ~~target~~ at least one inspection item.

3. (Currently Amended) The semiconductor circuit designing apparatus according to Claim 1, further comprising:

a layout design unit executing said layout design,

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit for which said layout design is executed, with regard to said ~~target~~ certain inspection item, and

wherein said circuit design unit provides a result of said inspection of said ~~target~~ semiconductor integrated circuit to said layout design unit.

4. **(Currently Amended)** The semiconductor circuit designing apparatus according to Claim 2, further comprising:

a layout design unit executing said layout design,

wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit for which said layout design is executed, with regard to said ~~target~~ certain inspection item, and

wherein said circuit design unit provides a result of said inspection of said ~~target~~ semiconductor integrated circuit to said layout design unit.

5. **(Currently Amended)** The semiconductor circuit designing apparatus according to Claim 4, wherein when said provided result of said inspection does not indicate a defect, said layout design unit stores said ID data of said circuit design unit and said number of times said circuit design unit failed said inspection of said ~~target~~ certain inspection item in said model development history database section.

6. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 1, wherein said inspection item database section is connected to said circuit design unit.

7. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 2, wherein said inspection item database section is connected to said circuit design unit.

8. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 3, wherein said inspection item database section is connected to said layout design unit.

9. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 4, wherein said inspection item database section is connected to said layout design unit.

10. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 5, wherein said inspection item database section is connected to said layout design unit.

11. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 3, wherein said layout design unit includes a plurality of layout design sections, and

wherein said inspection item database section is connected to at least one of said plurality of layout design sections.

12. **(Previously Presented)** The semiconductor circuit designing apparatus according to Claim 3, further comprising:

a data center distinct from said circuit design unit and said layout design unit,

wherein said inspection item database section is connected to said data center.

13. **(Currently Amended)** A semiconductor circuit designing method, comprising:

(a) providing an inspection item database section in which a circuit feature of a semiconductor integrated circuit for which a logical design should be executed corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed;

(b) notifying a circuit designer executing said logical design of said semiconductor integrated circuit of said inspection item, retrieved from said inspection

item database section, said inspection item corresponding to said circuit feature of said semiconductor integrated ~~circuit retrieved from said inspection item database section;~~ circuit; and

(c) executing said logical design of said semiconductor integrated circuit by said circuit designer with reference to said notified inspection item.

14. (Previously Presented) The semiconductor circuit designing method according to Claim 13, further comprising:

(d) providing said semiconductor integrated circuit for which said notified inspection item is satisfactory with a layout designer executing said layout design.

15. (Currently Amended) A semiconductor circuit designing method, comprising:

(a) providing a circuit design unit executing a logical design of a semiconductor integrated circuit; and

(b) providing an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to ~~an~~ at least one inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates ~~target~~ circuit feature information indicating said circuit feature ~~of a target semiconductor integrated circuit~~ of said semiconductor integrated circuit for which said logical design should be executed,

wherein said circuit design unit obtains a ~~target~~ certain inspection item of said at least one inspection item, said ~~target~~ certain inspection item corresponding to said ~~target~~ circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit with reference to said ~~target~~ certain inspection item.

16. **(Currently Amended)** A semiconductor circuit designing method, comprising:

(a) providing a circuit design unit executing a logical design of a ~~smeiconductor~~ semiconductor integrated circuit; and

(b) providing an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to ~~an~~ at least one inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed,

wherein said circuit design unit generates ~~target~~ circuit feature information indicating said circuit feature ~~of a target semiconductor integrated circuit~~ of said semiconductor integrated circuit for which said logical design should be executed,

wherein said circuit design unit obtains a ~~target~~ certain inspection item of said at least one inspection item, said ~~target~~ certain inspection item corresponding to said ~~target~~ circuit feature information from said inspection item database section, and

wherein said circuit design unit executes said logical design of said ~~target~~ semiconductor integrated circuit with reference to said ~~target~~ certain inspection item, and further comprising:

(c) providing a model development history database section in which ID data of said circuit design unit corresponds to a number of times said circuit design unit failed said inspection of each one of said at least one inspection item previously,

wherein said ~~target~~ certain inspection item is determined such that an inspection item of said at least one inspection item for which said number of times is smaller than a predetermined value is withdrawn from said ~~target~~ at least one inspection item.

17. (Currently Amended) The semiconductor circuit designing method according to Claim 15, further comprising:

~~(d)~~ (c) providing a layout design unit executing said layout design,

wherein said circuit design unit executes said inspection of said ~~target~~ semiconductor integrated circuit for which said layout design is executed, with regard to said ~~target~~ certain inspection item, and

wherein said circuit design unit provides a result of said inspection of said ~~target~~ semiconductor integrated circuit to said layout design unit.

18. (Currently Amended) The semiconductor circuit designing method according to Claim 16, further comprising:

~~(e)~~ (d) providing a layout design unit executing said layout design,

wherein said circuit design unit executes said inspection of said ~~target~~ semiconductor integrated circuit for which said layout design is executed, with regard to said ~~target~~ certain inspection item, and

wherein said circuit design unit provides a result of said inspection of said ~~target~~ semiconductor integrated circuit to said layout design unit.

19. (Currently Amended) The semiconductor circuit designing method according to Claim 18, wherein when said provided result of said ~~inspection,~~ inspection does not indicate a defect, said layout design unit stores said ID data of said circuit design unit and said number of times said circuit design unit failed said inspection of said ~~target~~ certain inspection item in said model development history database section.

20. (Previously Presented) The semiconductor circuit designing method according to Claim 15, wherein said inspection item database section is connected to said circuit design unit.